REMARKS

Claims 14-28 are pending in this application. By this Amendment, claims 14, 23 and 24 have been amended to further clarify the subject matter recited therein. Support for the amendments can be found, for example, at paragraphs [0055]-[0059]. Accordingly, no new matter has been added.

I. 35 U.S.C. §102 Rejection

The Office Action rejects claims 14-28 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,858,991 (hereinafter "Miyazawa").

Miyazawa fails to qualify as prior art under 35 U.S.C. §102(e). Miyazawa and the present application each list the same sole inventor. Therefore, Miyazawa is not "a patent granted on an application for patent **by another** filed in the United States before the invention by the applicant for patent" (emphasis added) as 35 U.S.C. §102(e) requires. Further, Miyazawa does not qualify as prior art under 35 U.S.C. §102(a) for similar reasons. Moreover, Miyazawa does not qualify as prior art under any other subsection of 35 U.S.C. §102.

Accordingly, withdrawal of the rejection is respectfully requested.

Notwithstanding the fact that Miyazawa fails to qualify as prior art under 35 U.S.C. §102, Applicant respectfully submits that Miyazawa, as well as each of the references from which Miyazawa claims priority, fails disclose each and every feature of independent claims 14 and 28. Specifically, Miyazawa and each of the references from which Miyazawa claims priority fail to disclose, teach or suggest at least "electrically connecting one of a source and a drain to the controlling terminal during a first period ... and supplying a driving current or a driving voltage to the electro-optical element during a second period, the source and the drain being electrically disconnected from the controlling terminal of the driving transistor during

at least part of the second period," (emphasis added) as recited by claim 14, and as similarly recited by claim 24.

Miyazawa discloses a pixel circuit including a driving transistor Tr1 and a compensating transistor Tr4 (see Fig. 2(a)). The gate of the driving transistor Tr1 is connected to the drain of the compensating transistor Tr4, the drain of the switching transistor Tr3, and one end of the capacitor C. Further, the compensating transistor Tr4 is a diode-connected transistor (i.e. the gate of transistor Tr4 is connected to the drain of Tr4). In an alternative embodiment shown in Fig, 2(b), the gate of driving transistor Tr1is connected to the source of the switching transistor Tr2.

In an alternative embodiment shown in Fig. 8, the gate of the driving transistor Trd is connected to the drain of the switching transistor Trs, one end of the capacitor C1, and the drain of the compensating transistor Trc. Transistor Trc is a diode-connected transistor (i.e. the gate of transistor Trc is connected to the drain of transistor Trc).

However, Miyazawa fails to disclose, teach or suggest electrically connecting one of a source and a drain to the controlling terminal of a driving transistor during a first period and electrically disconnecting the source and the drain from the controlling terminal during at least part of a second period, as recited by claim 14, and as similarly recited by claim 24. As noted above, Miyazawa discloses the drain of a compensating transistor (e.g. Tr4, Trc) connected to the gate of a driving transistor (e.g. Tr1, Trd). However, Miyazawa fails to disclose electrically disconnecting the drain and the gate. Further, Miyazawa discloses diode-connected transistors Tr4 and Trc in which the gate of the transistor is always connected to the drain of the transistor.

Therefore, Miyazawa fails to disclose "electrically connecting one of a source and a drain to the controlling terminal during a first period ... and the source and the drain being electrically disconnected from the controlling terminal of the driving transistor during at least

part of the second period," (emphasis added) as recited by claim 14, and as similarly recited by claim 24.

Further, Miyazawa fails to disclose "setting the potential of the controlling terminal to a second voltage level by using a capacitive coupling occurring at a capacitive element connected to the controlling terminal," as recited by claim 14, and as similarly recited by claim 24. All of the embodiments of the pixel circuit disclosed by Miyazawa include only a single capacitor. Thus, Miyazawa cannot disclose capacitive coupling.

Therefore, independent claims 14 and 24 are patentable. Claims 15-23 and 25-28 are also patentable for at least their dependency from claim 14 or claim 24 as well as for the additional features they recite.

II. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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JAO:SQV/hms

Attachment:
Request for Continued Examination

Date: April 24, 2008

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